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C. Barnes
6-20-01

EXPEDITED PROCEDURE - EXAMINING GROUP 2763

S/N 09/031,326 **PATENT**

entered
8/14/01 CC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Joseph J. Karniewicz	Examiner: Phan, T.
Serial No.:	09/031,326	Group Art Unit: 2763
Filed:	February 26, 1998	Docket: 303.376US1
Title:	PARAMETER POPULATION OF CELLS OF A HIERARCHICAL SEMICONDUCTOR STRUCTURE VIA FILE RELATION	

AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116

Box AF
Commissioner for Patents
Washington, D.C. 20231

In response to the Final Office Action mailed January 31, 2001, please amend the application as follows:

This response is accompanied by a Petition, as well as the appropriate fee, to obtain a one-month extension of the period for responding to the Office action, thereby moving the deadline for response from April 30, 2001 to May 31, 2001.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. Specific amendments to individual claims are detailed in the following marked up set of claims.

Please amend the claims as follows:

1. (Amended) A system for populating parameters of design cells defining the physical layout of a hierarchical semiconductor structure comprising:

a global file of global variables relating to layout of element blocks of the hierarchical semiconductor structure;

← Sel C1

a plurality of local files, each local file containing parameters relating a plurality of local variables to the global variables; and,

a plurality of programmable design cells, each cell corresponding to a local file and having a set of parameters [derived] created by relating the corresponding local variables within a local file to appropriate global values [in] from the global file such that changes of global